What is claimed is:

1. A method of reducing a channel length in a transistor, comprising:
forming a gate dielectric layer on a semiconductor substrate;
coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;
forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and
oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

2. The method of claim 1, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

3. The method of claim 2, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

4. The method of claim 2, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

5. The method of claim 1, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

6. The method of claim 1, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

7. A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

8. The method of claim 7, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

9. The method of claim 8, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

10. The method of claim 8, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

11. The method of claim 7, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

12. The method of claim 7, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

13. The method of claim 7, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

14. A method of forming a transistor, comprising:
forming a first source/drain region and a second source/drain region in a semiconductor substrate;
forming a gate dielectric layer on the semiconductor substrate;
coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;
forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides; and
oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

15. The method of claim 14, wherein coupling a nitride layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

16. The method of claim 15, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

17. The method of claim 15, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

18. The method of claim 14, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

19. The method of claim 14, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

20. The method of claim 14, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

21. A method of forming an integrated circuit, comprising:
forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:
forming a first source/drain region and a second source/drain region in the semiconductor substrate;
forming a gate dielectric layer on the semiconductor substrate;
coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;
forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;
oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and
electrically connecting the number of transistors.

22. The method of claim 21, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

23. The method of claim 22, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

24. The method of claim 22, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

25. The method of claim 21, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

26. The method of claim 21, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

27. A method of forming an integrated circuit, comprising:
forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:
forming a first source/drain region and a second source/drain region in the semiconductor substrate;
forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;
forming a gate dielectric layer on the semiconductor substrate;
coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;
forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;
oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and
electrically connecting the number of transistors.

28. A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

29. The method of claim 28, wherein coupling a nitride layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

30. The method of claim 29, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

31. The method of claim 29, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

32. The method of claim 28, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

33. The method of claim 28, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

34. The method of claim 28, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

35. A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of wordlines coupled to the first source/drain region of the number of transistors.

36. The method of claim 35, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

37. The method of claim 36, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

38. The method of claim 36, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

39. The method of claim 35, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

40. The method of claim 35, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

41. A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of wordlines coupled to the first source/drain region of the number of transistors.

42. A method of making an information handling system, comprising:

providing a processor chip;

forming a semiconductor memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors;

forming a number of wordlines coupled to the first source/drain region of the number of transistors; and

coupling the processor chip to the semiconductor memory device with a system bus.

43. The method of claim 42, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

44. The method of claim 43, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate dielectric layer to form a silicon nitride (SiN) layer.

45. The method of claim 43, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises composite oxidation processing the gate dielectric layer to form a silicon nitride (SiN) layer.

46. The method of claim 42, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

47. The method of claim 42, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

48. The method of claim 42, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

49. A transistor comprising:

a first source/drain region and a second source/drain region disposed in a substrate;

a channel region between the first source/drain region and the second source/drain region;

a gate dielectric layer coupled to the channel region;

a barrier layer coupled to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

a gate formed from a gate material coupled to the barrier layer; and

a side dielectric region converted from a portion of the gate material, the side dielectric region having a thickness at a top of the gate that is substantially the same as a thickness at a bottom of the gate.

50. The transistor of claim 49, wherein the barrier layer comprises a nitrided layer.

51. The transistor of claim 50, wherein the nitrided layer comprises silicon nitride.

52. The transistor of claim 50, wherein the side dielectric region comprises silicon dioxide.

53. The transistor of claim 50, further comprising a source/drain extension operatively connected to the first source/drain region extending into the channel region.

54. A transistor formed by the following process:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides,

and an effective channel length defined by the sides; and

oxidizing the gate wherein a portion of the sides of the gate are converted to

an oxide and an effective channel length of the gate is reduced.